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EXAMINER	
LAI, VINCENT	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/685,654	Applicant(s) RUPLEY ET AL.	
	Examiner Vincent Lai	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2007*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21,24-46,48,49 and 51-53* is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-21,24-46,48,49 and 51-53* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☐ All b)☐ Some * c)☐ None of:
1.☐ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 January 2007 has been entered.

Response to Amendment

2. Objection to the specification and claims are withdrawn after considering amendments.

3. The 35 USC 112 rejection is withdrawn after considering explanation found in the remarks.

Response to Arguments

4. Applicant's arguments with respect to claims 1-21, 24-46, and 51-53 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-7, 12, 16, 19, 21, 24-26, 28, 29, 37-41, 46, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by Poplingher et al (U.S. Patent # 6,871,275 B1), herein referred to as Poplingher, in view of the Examiner's use of Official Notice.

As per **claim 1**, Poplingher discloses an apparatus comprising:

a micro-operation generator (See figure 3: Decoder 106) to receive a predicated instruction that indicates a plurality of destination registers (See column 3, lines 44-47: Decoding specifies a register out of the GPR file);

the micro-operation generator further to generate a plurality of micro-operations that implement the instruction (See column 3, lines 41-44: The decoder decodes instructions into micro-operations);

the micro-operation generator further to decompose the predicated instruction into the plurality of micro-operations that implement the instruction such that at least one of the plurality of micro-operations indicate a single destination register that is distinct form the destination registers indicated by other micro-operations (See column 8, line 17-21: A predicate branch target address is saved in a separate register).

As per **claim 2**, Poplingher discloses the apparatus of claim 1, wherein

the plurality of micro-operations includes one or more standard micro-operations to provide the basic functionality indicated by the instruction (See column 3, lines 41-44: The decoder decodes instructions into micro-operations).

As per **claim 3**, Poplingher discloses the apparatus of claim 1, wherein

the plurality of micro-operations includes one or more predication-support micro-operations (See column 3, lines 41-44: The decoder decodes instructions into multiple micro-operations).

As per **claim 4**, Poplingher discloses the apparatus of claim 3, wherein:

the one or more predication-support micro-operations includes a conditional move micro-operation for each destination register indicated by the instruction where the conditional move micro-operation is to select between a first and second proposed output value based on the value of a qualifying predicate associated with the instruction (See column 7, lines 37-52: A determination and selection is made with predication).

As per **claim 5**, Poplingher discloses the apparatus of claim 4, wherein:

the first proposed output value is the incoming value of the associated destination register (See column 7, lines 37-52: This would be the no branch value) and the second proposed output value is a computed value (See column 7, lines 37-52: A compare instruction would compute a value to store in the predicate register).

As per **claim 6**, Poplingher discloses the apparatus of claim 4, wherein:

the first proposed output value is the incoming value of the associated destination register (See column 7, lines 37-52: This would be the no branch value); and the second proposed output value is a constant value (See column 6, lines 54-61: When a prediction is unavailable).

As per **claim 7**, Poplingher discloses the apparatus of claim 6, wherein the instruction is a compare instruction (See column 7, lines 37-52: CMP is compare).

As per **claim 12**, Poplingher discloses the apparatus of claim 4, wherein:

the instruction is a parallel compare instruction (See column 3, lines 11-13 and column 7, lines 37-52: A compare instruction is used and instructions are run in parallel).

As per **claim 16**, Poplingher discloses the apparatus of claim 3, wherein:

the one or more predication support micro-operations includes an append operation to append a qualifying predicate value to a proposed output value (See column 7, lines 37-52: Predication updates the predicate register).

As per **claim 19**, Poplingher discloses a system comprising:

a memory to store an instruction that indicates a plurality of destination registers (See column 3, lines 44-47 and column 4, lines 15-21: Decoding specifies a register out of the GPR file. Instructions are stored in a memory device); and

a processor coupled to the memory (See figure 3: Processor 101 and Memory 124);

wherein the processor includes a microcode engine to generate (See column 3, lines 41-44: The decoder decodes instructions into micro-operations), for the instruction, at least:

a first micro-operation to associate a predicate value with a first value from a first register in a second register, the second register being different from the first register (See column 8, line 17-21: A predicate branch target address is saved in a separate register),

a second micro-operation to store a second value in the first register (See column 7, lines 37-52: Storing of predicate values is done), and

a select micro-operation to select the first or second value to be stored in the first register based on the predicate value associated with the first value in the second register (See column 7, lines 37-52: A determination and selection is made with predication).

As per **claim 21**, Poplingher discloses the system of claim 19, wherein:

The select a micro-operation includes a conditional move micro-operation to conditionally move the first value or the second value into the first register based on the predicate value associated with the first value in the second register (See column 7, lines 37-52: A determination and selection is made with predication).

As per **claim 24**, Poplingher discloses a method comprising:

receiving an instruction that indicates a plurality of destination registers (See column 3, lines 44-47: Decoding specifies a register out of the GPR file); and

generating a plurality of standard micro-operations for the instruction, (See column 3, lines 41-44: The decoder decodes instructions into micro-operations) wherein at least one of the plurality of standard micro-operations indicates a single destination register that is distinct from the destination registers indicated in the other standard micro-operations of the plurality of standard micro-operations (See column 8, line 17-21: A predicate branch target address is saved in a separate register).

As per **claim 25**, Poplingher discloses the method of claim 24, further comprising: generating, if the instruction is predicated, a plurality of predication-support micro-operations for the instruction (See column 3, lines 41-44: The decoder decodes instructions into multiple micro-operations).

As per **claim 26**, Poplingher discloses the method of claim 25, wherein generating a plurality of predication-support micro-operations further comprises: generating a conditional move micro-operation for each destination register indicated by the instruction (See column 7, lines 37-52: A determination and selection is made with predication).

As per **claim 28**, Poplingher discloses the method of claim 26, wherein generating a conditional move operation further comprises:

if the instruction does not indicate a known constant as a potential output value, generating a micro-operation that receives a first potential output value as an input and also receives a second potential output value as an input (See column 6, lines 54-61: When a prediction is unavailable), wherein execution of the micro-operation is to cause a processor to move either the first potential output value or the second potential output value into a destination register (See column 7, lines 37-52: A determination and selection is made with predication).

As per **claim 29**, Poplingher discloses the method of claim 25, wherein generating a plurality of predication-support micro-operations further comprises:

generating an append micro-operation for reach destination register indicated by the instruction, wherein execution of the micro-operation is to cause a processor to append a qualifying predicate for the instruction with a potential output value, and is to further cause the appended value to be stored in a register (See column 7, lines 37-52: Predication updates the predicate register).

As per **claim 37**, Poplingher discloses the apparatus of claim 30, wherein the second value includes a result of a standard micro-operation to provide the basic functionality indicated by the predicated instruction (See column 3, lines 41-44: The decoder decodes instructions into micro-operations).

As per **claim 38**, Poplingher discloses the apparatus of claim 30, wherein the first value comprises the predication value appended to an incoming value from the second register (See column 7, lines 37-52: Predication updates the predicate register).

As per **claim 39**, Poplingher discloses the apparatus of claim 30, wherein: the third micro-operation includes a conditional move micro-operation to select the first value or the second value to be moved to the second destination register based on the predication value (See column 7, lines 37-52: A determination and selection is made which then moves values).

As per **claim 40**, Poplingher discloses the apparatus of claim 39, wherein: the first value is an incoming value of the second destination register; and the second value is a computed value (See column 7, lines 37-52: A compare instruction would compute a value to store in the predicate register).

As per **claim 41**, Poplingher discloses the apparatus of claim 39, wherein: the first value is an incoming value of the second destination register; and the second value is a constant value (See column 6, lines 54-61: When a prediction is unavailable).

As per **claim 46**, Poplingher discloses the apparatus of claim 31, wherein:

The predicated instruction is a parallel compare instruction (See column 3, lines 11-13 and column 7, lines 37-52: A compare instruction is used and instructions are run in parallel).

As per **claim 53**, Poplingher discloses the apparatus of claim 30, wherein: the micro-operation generator is further to decompose the instruction into the plurality of micro-operations such that each of the micro-operations indicates a single destination register (See column 3, lines 41-44: The decoder decodes instructions into micro-operations).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8-11, 20, 30-36, and 42-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poplingher et al (U.S. Patent # 6,871,275 B1), herein referred to as Poplingher, in view of the Examiner's use of Official Notice.

[Examiner's Note: The Examiner is relying on the disclosure of a compare instruction, see rejection of claim 7, and official notice for the rejections of claims 8-11. It is the determination of the Examiner that the various manners in which a compare instruction can take form, as claimed by the Applicant, is well-known prior art. See MPEP 2144.03]

As per **claim 8**, Poplingher discloses the apparatus of claim 7, wherein the instruction is an "or" form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "or" form compare instruction).

As per **claim 9**, Poplingher discloses the apparatus of claim 7, wherein the instruction is an "and" form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "and" form compare instruction).

As per **claim 10**, Poplingher discloses the apparatus of claim 7, wherein the instruction is an "and"-complement form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "and"-complement form compare instruction).

As per **claim 11**, Poplingher discloses the apparatus of claim 7, wherein the instruction is an "or"-complement form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "or"-complement form compare instruction).

[Examiner's Note: The Examiner is relying on the disclosure of a memory, see rejection of claim 19, and official notice for the rejections of claims 20. It is the determination of the Examiner that the various forms in which a memory can take, as claimed by the Applicant, is well-known prior art. See MPEP 2144.03]

As per **claim 20**, Poplingher discloses the system of claim 19, wherein:

the memory is a DRAM (See figure 3: Memory 124)

[Examiner's Note: The Examiner is relying on the disclosure of instructions, see column 3, lines 41-49, and official notice for the rejections of claims 30-36. It is the determination of the Examiner that the various manners in which an instruction can take form, as claimed by the Applicant, is well-known prior art. See MPEP 2144.03]

As per **claim 30**, Poplingher discloses an apparatus comprising:

a micro-operation generator to receive a predicated instruction (See figure 3: Decoder 106), the predicated instruction being one of a plurality of instructions (See column 3, lines 41-49: The predicated instruction may belong to any number fetched), the plurality of instructions to include arithmetic instructions and memory instructions (See column 3, lines 41-49: Arithmetic and memory instructions are well known in the art);

the micro-operation generator further to generate a plurality of micro-operations that implement the instruction (See column 3, lines 41-44: The decoder decodes instructions into micro-operations) wherein the plurality of micro-operations include

a first micro-operation to store a first value in a first destination register (See column 8, line 17-21: Predicate branch target address is saved in separate registers),

a second micro-operation to store a second value in a second destination register, which is different from the first destination register (See column 8, line 17-21: A Predicate branch target address is saved in separate registers), and a third micro-operation to select the first value or the second value to be stored in the second destination register based on a predication value (See column 7, lines 37-52: A determination and selection is made which then moves values).

As per **claim 31**, Poplingher discloses the apparatus of claim 30, wherein the predicated instruction is an arithmetic instruction (See column 3, lines 41-49: Arithmetic instructions are well known in the art).

As per **claim 32**, Poplingher discloses the apparatus of claim 31, wherein the predicated instruction is an add instruction (See column 3, lines 41-49: Add instructions are well known in the art).

As per **claim 33**, Poplingher discloses the apparatus of claim 31, wherein the predicated instruction is a compare instruction (See column 7, lines 37-52: A compare instruction is taught).

As per **claim 34**, Poplingher discloses the apparatus of claim 30, wherein the predicated instruction is a memory instruction (See column 3, lines 41-49: Memory instructions are well known in the art).

As per **claim 35**, Poplingher discloses the apparatus of claim 34, wherein the predicated instruction is a load instruction (See column 3, lines 41-49: Load instructions are well known in the art).

As per **claim 36**, Poplingher discloses the apparatus of claim 34, wherein the predicated instruction is a store instruction (See column 3, lines 41-49: Store instructions are well known in the art).

[Examiner's Note: The Examiner is relying on the disclosure of a compare instruction, see rejection of claim 33, and official notice for the rejections of claims 42-45. It is the determination of the Examiner that the various manners in which a compare instruction can take form, as claimed by the Applicant, is well-known prior art. See MPEP 2144.03]

As per **claim 42**, Poplingher discloses the apparatus of claim 33, wherein the predicated instruction is an "or" form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "or" form compare instruction).

As per **claim 43**, Poplingher discloses the apparatus of claim 33, wherein the predicated instruction is an "and" form compare instruction (See column 7, lines 37-52:

CMP is compare. It is well known in the art as to how to use an "and" form compare instruction).

As per **claim 44**, Poplingher discloses the apparatus of claim 33, wherein the predicated instruction is an "and"-complement form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "and"-complement form compare instruction).

As per **claim 45**, Poplingher discloses the apparatus of claim 33, wherein the predicated instruction is an "or"-complement form compare instruction (See column 7, lines 37-52: CMP is compare. It is well known in the art as to how to use an "or"-complement form compare instruction).

7. Claims 13-15, 27, 48, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poplingher in view of Intel ("Intel® Itanium™ Architecture Software Developer's Manual", Volume 1: Application Architecture, Revision 2.0, December 2001).

As per **claim 13**, Poplingher disclose the limitations as stated in **claim 12.**

Intel also discloses the apparatus of claim 12, wherein: the one or more predication-support micro-operations include a first conditional move micro-operation for a first destination register indicated by the parallel compare instruction; the one or more predication-support micro-operations also include a second conditional move micro-operation for a second destination register indicated by the parallel compare instruction; the first proposed output value for the first conditional move micro-operation is the incoming value of the associated destination register; the second proposed output value for the first conditional move micro-operation is a first constant; the first proposed output value for the second conditional move micro-operation is the incoming value of the associated destination register; the second proposed output value for second first conditional move micro-operation is a second constant (See Intel, §4.3.1, lines 1-4; (Examiner's note: In this citation, Intel discloses the basic concept of predication wherein, depending on a predicate value, either an instruction is passed or a constant value (NOP) is passed, thus illustrating the concept of passing an argument or a constant); §4.3.3, lines 16-19 (In this citation, Intel discloses a DeMorgan-type compare function which essentially gates using two predicates, thus, in conjunction with the previous cite illustrates the use of two conditional move instructions passing either an instruction or a constant).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 14**, Poplingher and Intel disclose the limitations as stated in **claim 13**.

Intel further discloses the instruction [being] an "and.orcm" form of a parallel compare instruction (See Intel, Table 4-9, Compare Type: DeMorgan, Completer: and.orcm).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 15**, Poplingher and Intel disclose the limitations as stated in **claim 13**.

Intel further discloses the instruction [being] an "or.andcm" form of a parallel compare instruction (See Intel, Table 4-9, Compare Type: DeMorgan, Completer: or.andcm).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 27**, Poplingher discloses the limitations as stated in **claim 26**.

Poplingher does not explicitly disclose *if the instruction indicates a known constant as a first potential output value, generating a micro-operation that receives a second potential output value as an input, wherein execution of the micro-operation is to cause a processor to move either the constant value or a second potential output value into a destination register* (See Intel, §4.3.1, lines 1-4; Examiner's note: In this citation, Intel discloses outputting either an instruction or a NOP (no instruction, which is viewed as a constant value)).

As per **claim 48**, Poplingher and Intel disclose the limitations as stated in **claim 46**.

Intel further discloses *the instruction* [being] *an "and.orcm" form of a parallel compare instruction* (See Intel, Table 4-9, Compare Type: DeMorgan, Completer: and.orcm).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 49**, Poplingher and Intel disclose the limitations as stated in **claim 46**.

Intel further discloses *the instruction* [being] *an "or.andcm" form of a parallel compare instruction* (See Intel, Table 4-9, Compare Type: DeMorgan, Completer: or.andcm).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

8. Claims 17, 18, 51, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poplingher in view of Dulong ("The IA-64 Architecture at Work", Carol Dulong, Intel Corp., 1998).

As per **claim 17**, Poplingher discloses the limitations as stated in **claim 3**.

Poplingher does not explicitly disclose the instruction [being] a load instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a load address.

Dulong does disclose the instruction [being] a load instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a load address (See page 1, column 1, lines 30-32: Dulong discloses appending a predicate to all instructions, including load instructions).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 18**, Poplingher discloses the limitations as stated in **claim 3**.

Poplingher does not explicitly disclose the instruction [being] a store instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a store address.

Dulong does disclose the instruction [being] a store instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a store address (See page 1, column 1, lines 30-32; Examiner's note: Dulong discloses appending a predicate to all instructions, including store instructions).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 51**, Poplingher discloses the limitations as stated in **claim 30**.

Poplingher does not explicitly disclose the predicated instruction [being] a load instruction; and the first micro-operation [including] an append operation to append the predication value to a load address.

Dulong does disclose the instruction [being] a load instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a load address (See page 1, column 1, lines 30-32: Dulong discloses appending a predicate to all instructions, inherently including a load instruction).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

As per **claim 52**, Poplingher discloses the limitations as stated in **claim 30**.

Poplingher does not explicitly disclose the predicated instruction [being] a store instruction; and the first micro-operations [including] an append operation to append predication value to a store address.

Dulong does disclose the instruction [being] a store instruction; and the one or more predication support micro-operations [including] an append operation to append a qualifying predicate value to a store address (See page 1, column 1, lines 30-32;

Examiner's note: Dulong discloses appending a predicate to all instructions, inherently including a load instruction).

The advantage of utilizing a instruction set similar to that of the Intel instruction set at the time of invention would have been to utilize a well-known and tested instruction set architecture which allows for predication support. This advantage would have motivated one of ordinary skill in the art at the time of invention to utilize an instruction set that would be similar in spirit to modern processors at the time invention, such as the IA-64. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a current instruction set within the invention disclosed by Poplingher.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent Lai
Examiner
Art Unit 2181

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April 4, 2007

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DONALD SPARKS
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